INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number: DN0382921

□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: N070ICE-G02 (C1)

Product ID：GN070ICE0010S

Customer: Asus

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note :

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
陳鵲如	張智勝	季維康

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Mar., 26, 2014	All	Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N070ICE-G02 is a 7" (7" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 31 pins MIPI interface. This module supports 800 x 1280 WXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	7" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 1280	pixel	-
Pixel Pitch	0.11775 (H) x 0.11775 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White	400	Cd/m2	
Power Consumption	1.6 W (Max.) (Panel 0.4 W (Max.), BLU 1.2W (Max.))		(1)

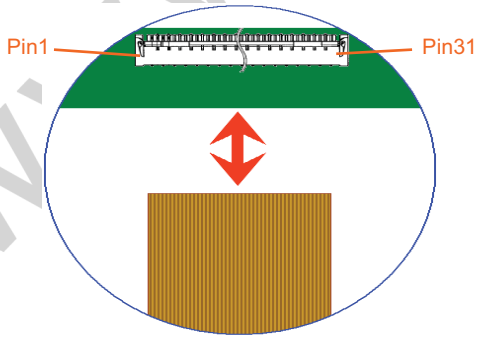
Note (1) The specified power consumption (without LED converter efficiency) is under the conditions at **VCI = 3.3 V, VDDI= 1.8V, fv = 60 Hz, Brightness = 400nits, I_{F_LED} = 20mA** and Ta = 25 ± 2 ºC, whereas **white** pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	103.3	103.5	103.7	mm	(1)
	Vertical (V)	162.02	162.22	162.42	mm	
	Thickness (T)			2.65 (w/o PCBA) 4.51 (w/ PCBA)	mm	
Bezel Area (CF Polarizer)	Horizontal	97.15	97.35	97.55	mm	
	Vertical	153.62	153.82	154.02	mm	
Active Area	Horizontal		94.2		mm	
	Vertical		150.72		mm	
Weight		-	-	88	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer to Appendix Outline Drawing for detail design.

Connector Part No.: **Panasonic AYF333135 or Equivalent**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

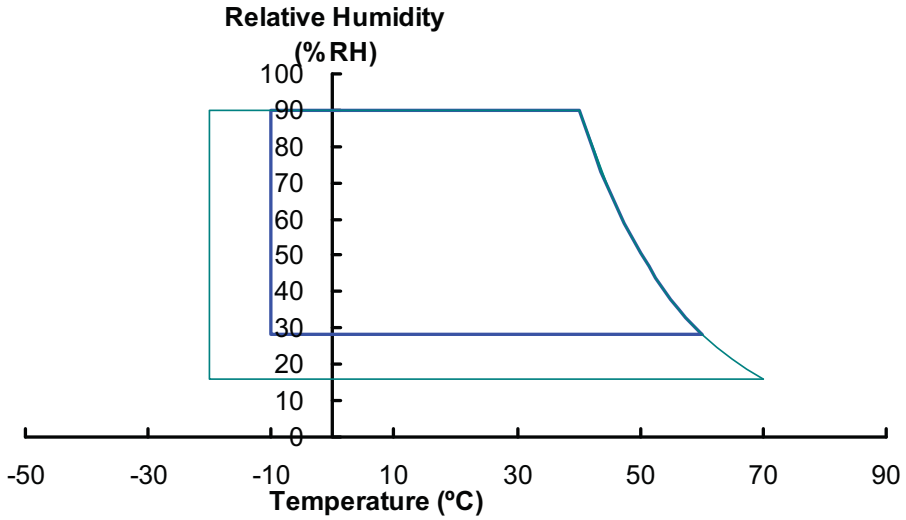
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 70 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

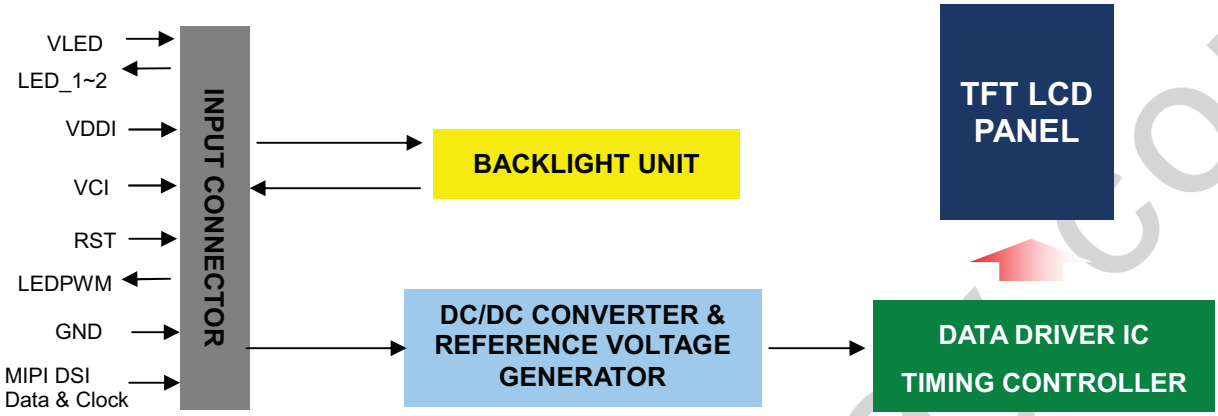
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCI	-0.3	+5.0	V	(1)
	VDDI	-0.3	+2.0	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

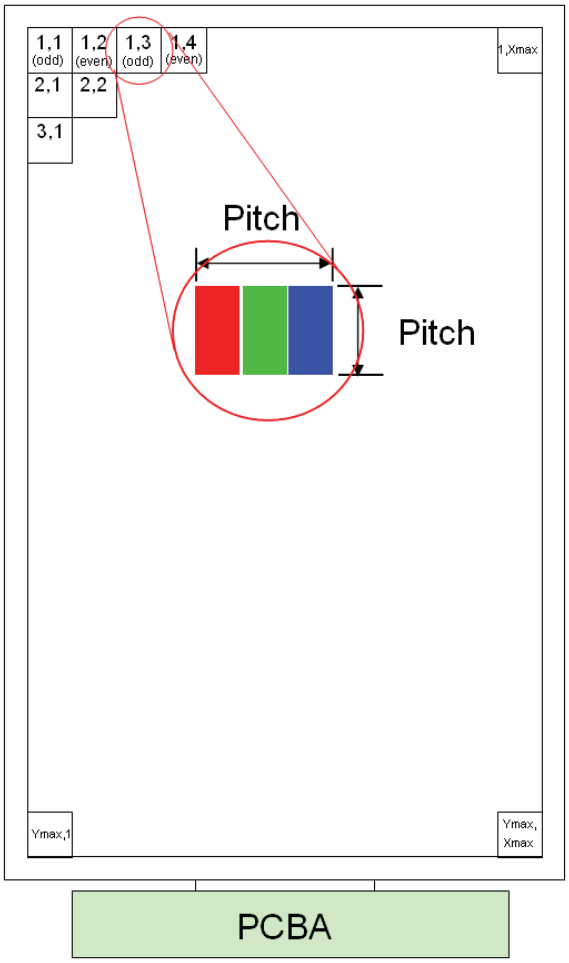
Pin	Symbol	I/O	Description	Remark
1	GND	P	Ground	
2	D3_P	I	MIPI differential data3 input (Positive)	
3	D3_N	I	MIPI differential data3 input (Negative)	
4	GND	P	Ground	
5	D2_P	I	MIPI differential data2 input (Positive)	
6	D2_N	I	MIPI differential data2 input (Negative)	
7	GND	P	Ground	
8	CLK_P	I	MIPI differential clock input (Positive)	
9	CLK_N	I	MIPI differential clock input (Negative)	
10	GND	P	Ground	
11	D1_P	I	MIPI differential data1 input (Positive)	
12	D1_N	I	MIPI differential data1 input (Negative)	
13	GND	P	Ground	
14	D0_P	I	MIPI differential data0 input (Positive)	
15	D0_N	I	MIPI differential data0 input (Negative)	
16	GND	P	Ground	
17	RST	I	Device reset signal	1.7V~1.9V
18	VCI	P	3.3V input	3.0V~3.6V
19	VCI	P	3.3V input	3.0V~3.6V
20	NC			
21	VDDI	P	1.8V input	1.7V~1.9V

22	VDDI	P	1.8V input	1.7V~1.9V
23	ID		Ground	
24	GND	P	Ground	
25	LEDPWM	O	PWM control signal for LED driver (CABC)	1.7V~1.9V
26	GND	P	Ground	
27	LED	P	Cathode for light bar	
28	LED	P	Cathode for light bar	
29	NC(MTP)	P	No connection, please keep it floating	
30	VLED	P	Anode for light bar	9V~10V
31	VLED	P	Anode for light bar	9V~10V

Note (1) The first pixel is odd as shown in the following figure.

Note (2) Normal operation/BIST pattern selection. (Control by MIPI LP Command)

Note (3) The LCD only supports one-way scanning.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELECTRICAL SPECIFICATION

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power Supply Voltage		VCI	3.0	3.3	3.6	V	
		VDDI	1.7	1.8	1.9	V	
VDDI High Level Input Voltage		V_{IH2}	0.7 VDDI	-	VDDI	V	For I/O circuit
VDDI Low Level Input Voltage		V_{IL2}	0	-	0.3 VDDI	V	
Power Supply Current	White	I_{VCI}		65	90	mA	Note (2)
		I_{VDDI}		35	55	mA	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) The specified power supply current is under the conditions at VCI = 3.3 V, VDDI = 1.8 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power-dissipation check pattern is displayed below.

White Pattern

Active Area

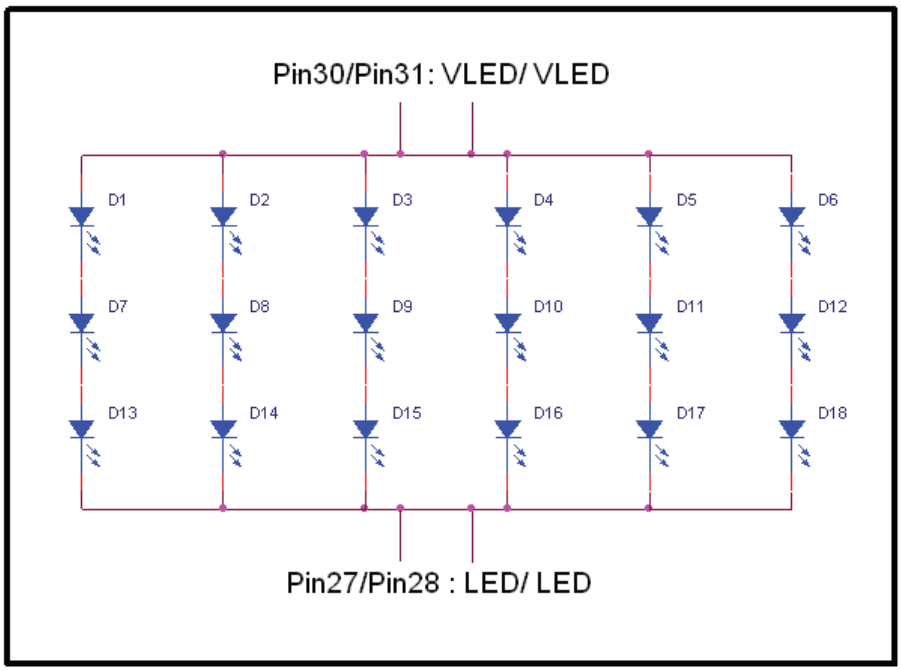
4.3.2 LED CONVERTER SPECIFICATION

N/A

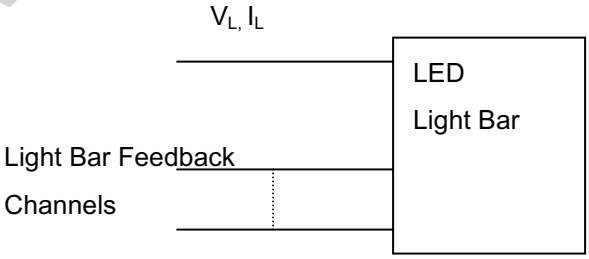
4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	VL	7.8	8.7	9.6	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	IL	-	120	-	mA	
Power Consumption	PL	-	1.05	1.2	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)



Note (1) LED current is measured by utilizing a high frequency current meter as shown below :

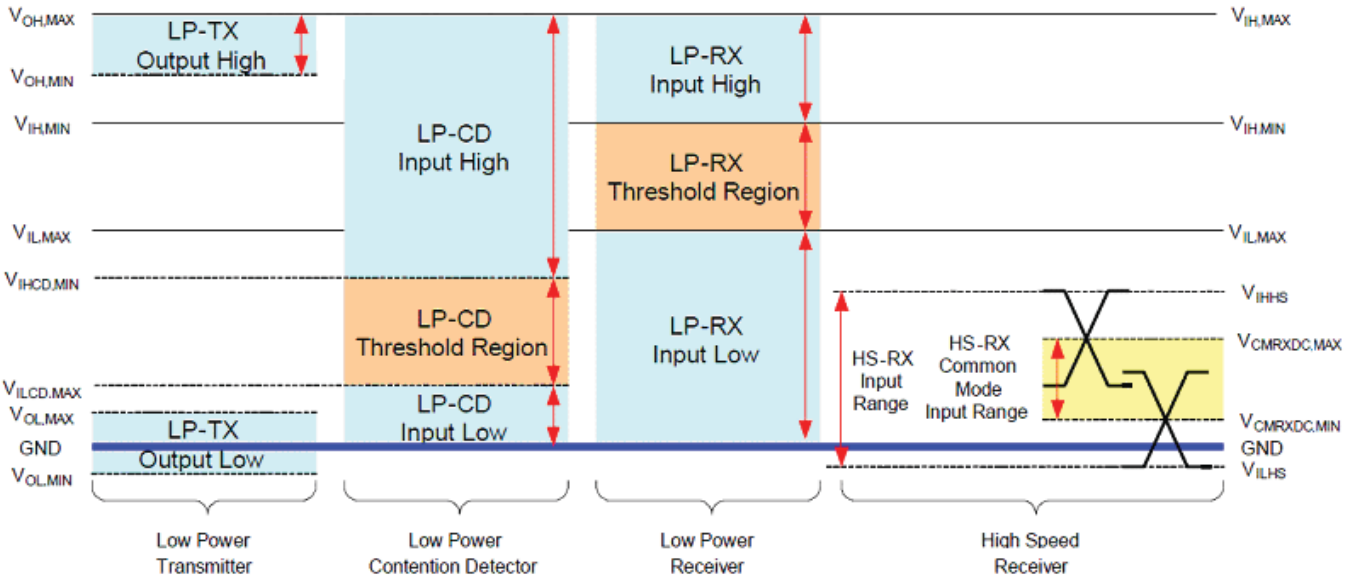


Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The life time of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

4.4 MIPI DSI INPUT SIGNAL TIMING SPECIFICATIONS



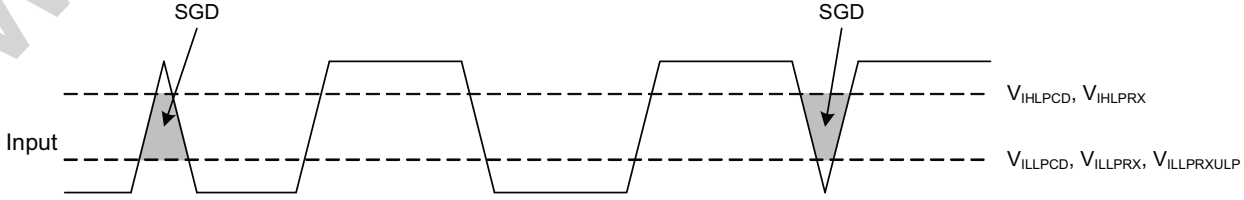
MIPI DC Diagram

4.4.1 DC Electrical Characteristic

4.4.1.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	VIHLPCD	LP-CD	450	-	1350	mV
Logic low level input voltage	VILLPCD	LP-CD	0	-	200	mV
Logic high level input voltage	VIHLPRX	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	VILLPRX	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	VILLPRXULP	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	VOHLPTX	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	VOLLPTX	LP-TX (D0)	-50	-	50	mV
Logic high level input current	IIH	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	IIL	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) **VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)**
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

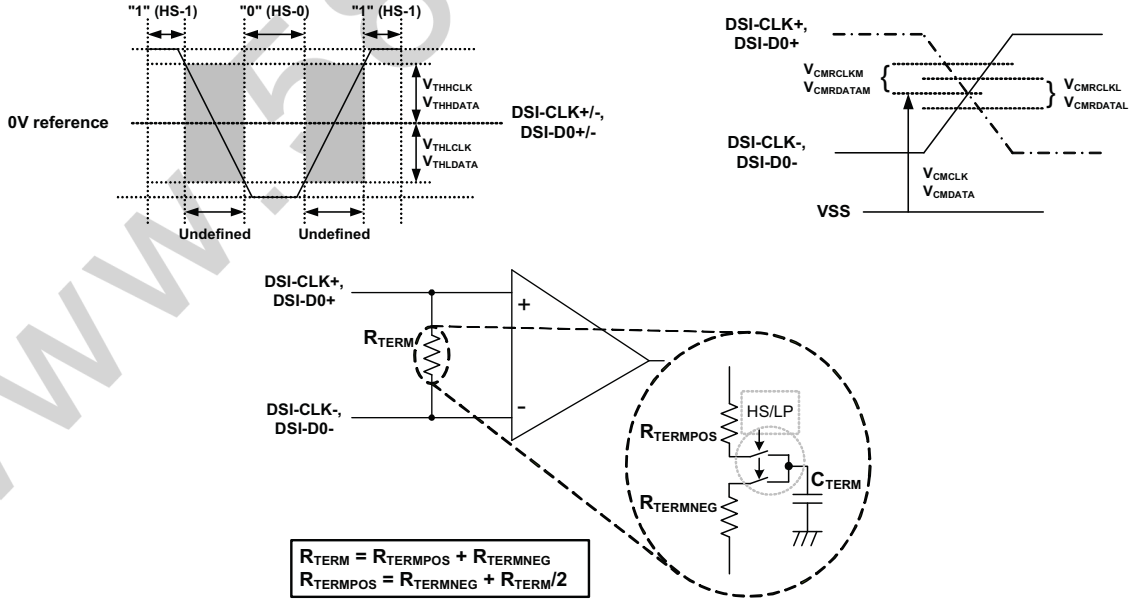


Spike/Glitch rejection-DSI

4.4.1.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) **VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V**, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM .
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

4.4.2 AC Electrical Characteristics

4.4.2.1 MIPI DSI Timing Characteristics

4.4.2.1.1 High Speed Mode

(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*** ,Ta = -30 to 70℃)

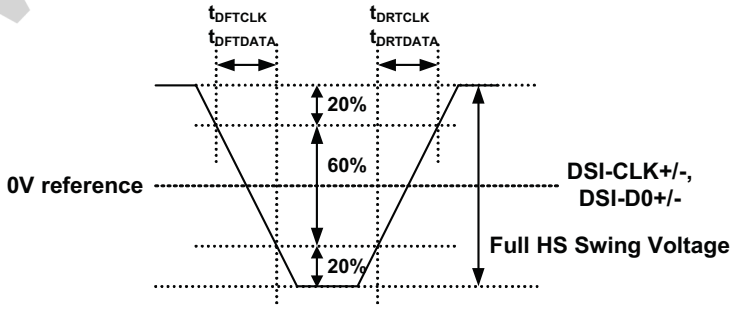
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.

DSI clock channel timing

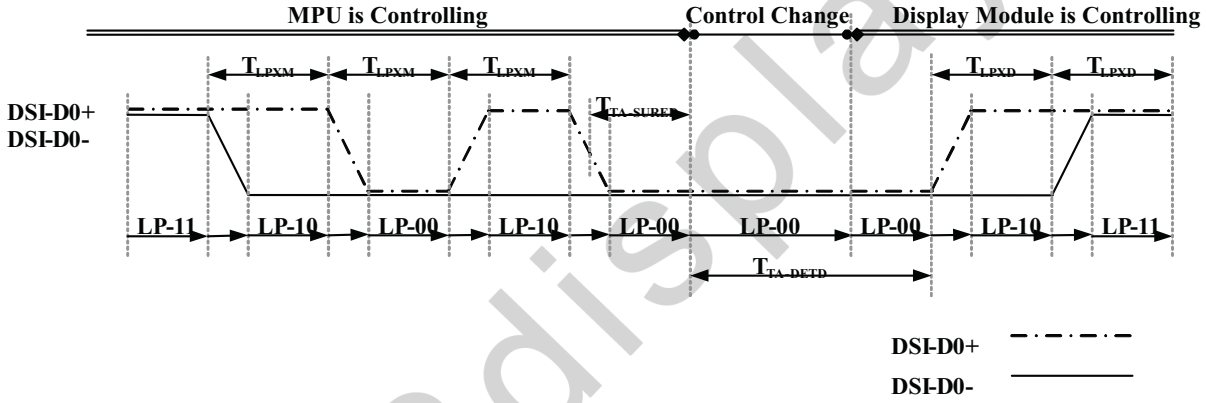


Rising and fall time on clock and data channel

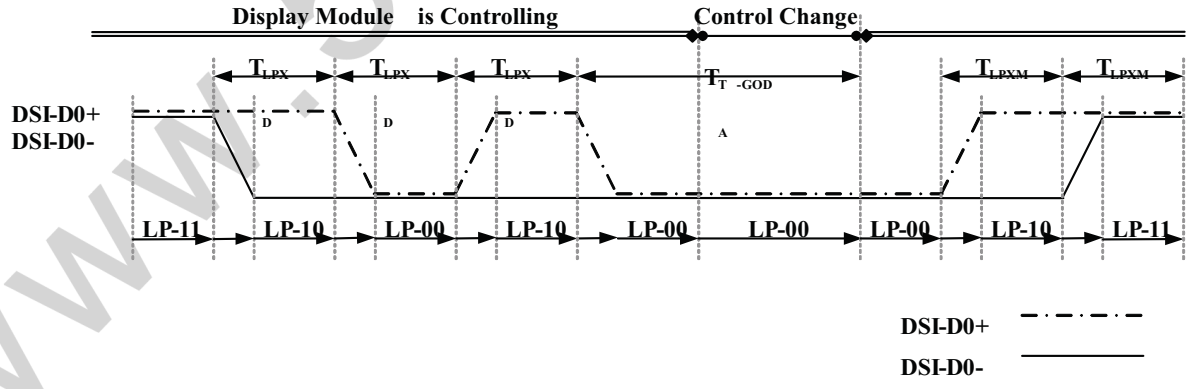
4.4.2.1.2 Low Power Mode

(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,***Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output



Bus Turnaround (BTA) from MPU to display module Timing



Bus Turnaround (BTA) from display module to MPU Timing

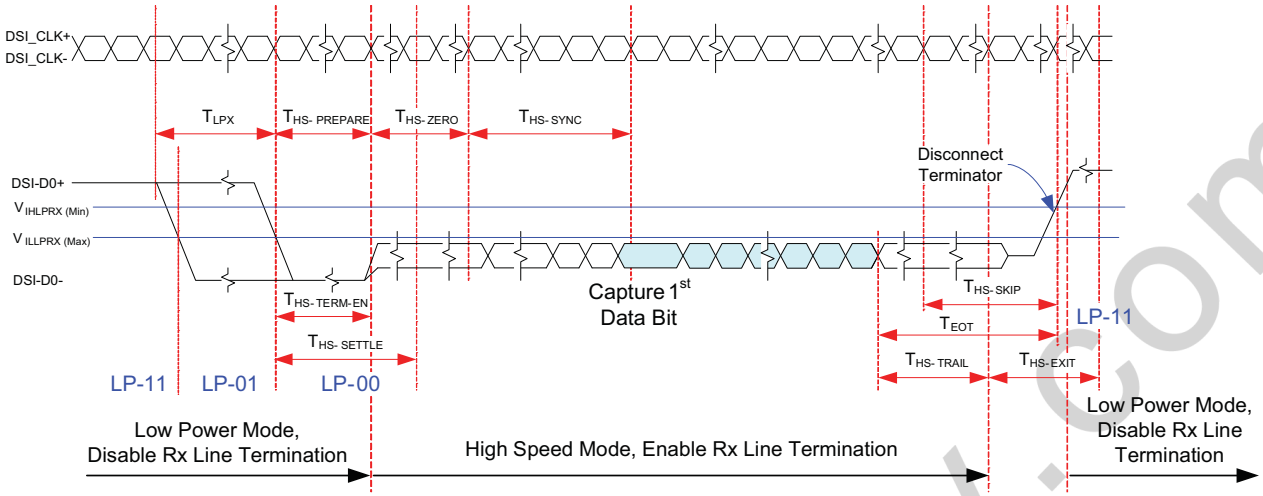
4.4.2.1.3 DSI Bursts

(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,***Ta = -30 to 70℃)

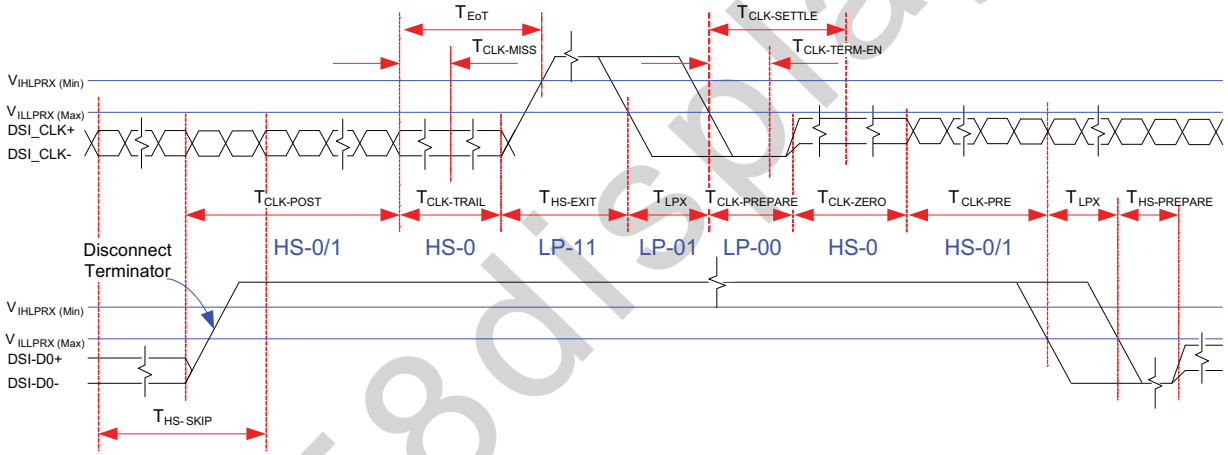
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4x UI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4x UI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52 xUI	-	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

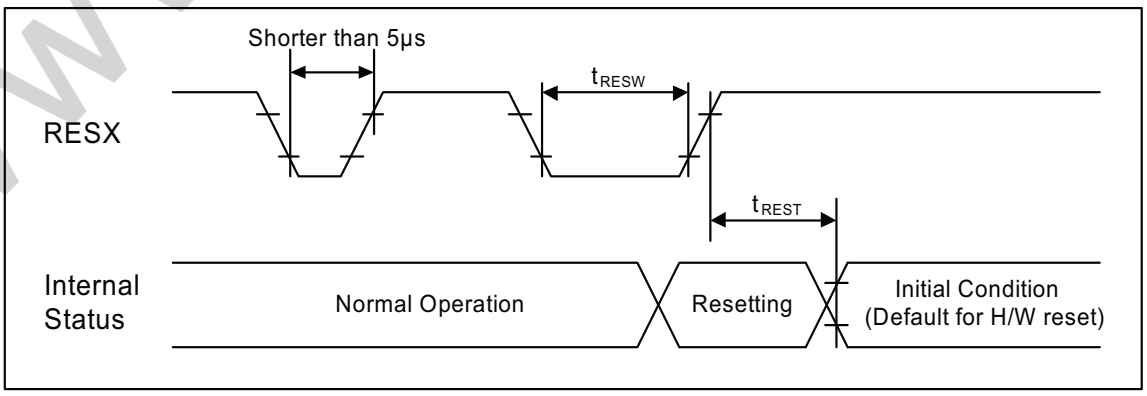


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

4.4.2.2 Reset Input Timing



Reset input timing

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	μs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

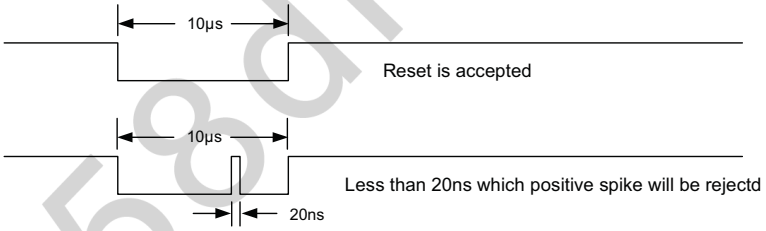
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

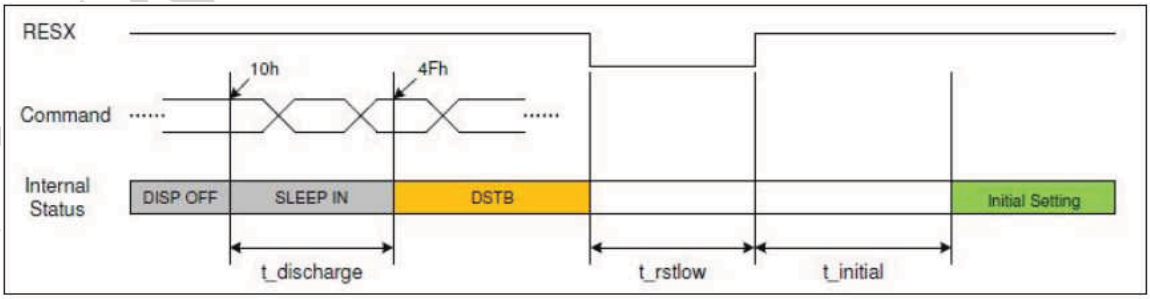
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

4.4.2.3 Deep Standby Mode Timing



(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V***,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tdischarge	Sleep in into DSTB delay time	-	-	100	ms	
	trstlow	Reset low pulse	3	-	-	ms	
	tinitial	Reset high to initial setting delay time	-	-	120	ms	

Note 1) t_discharge suggested delay time over 100ms.

Note 2) t_initial suggested delay time over 120ms..

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.
DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

4.5.1 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.

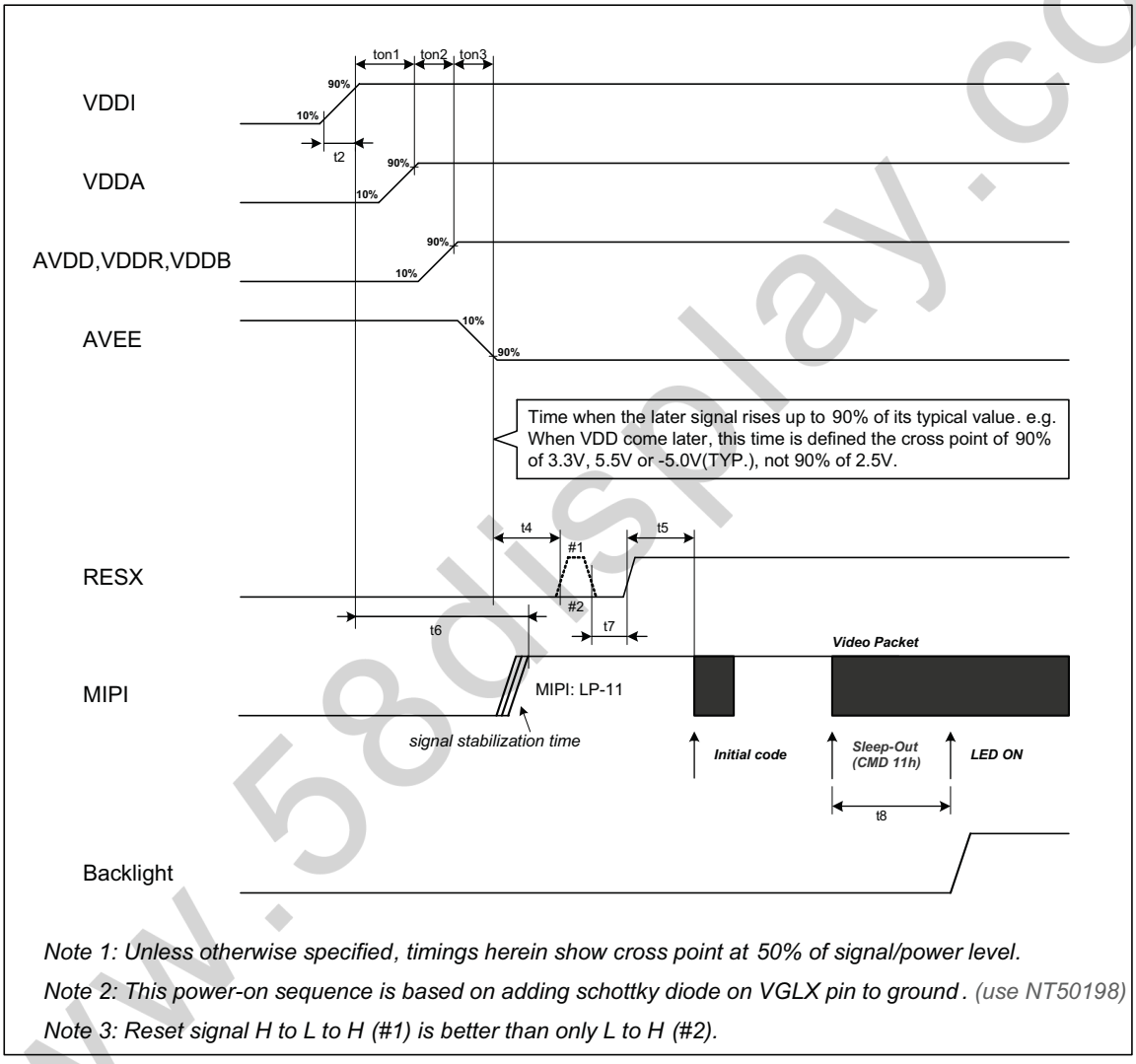
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

a. Power on:

VDDI (V18)=1.7~1.9V, VDDA (V33)= 3.0~3.6V ;

The sequences of AVDD=4.5~6.0V and AVEE=-4.5~-6.0V are only for reference



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground. (use NT50198)

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

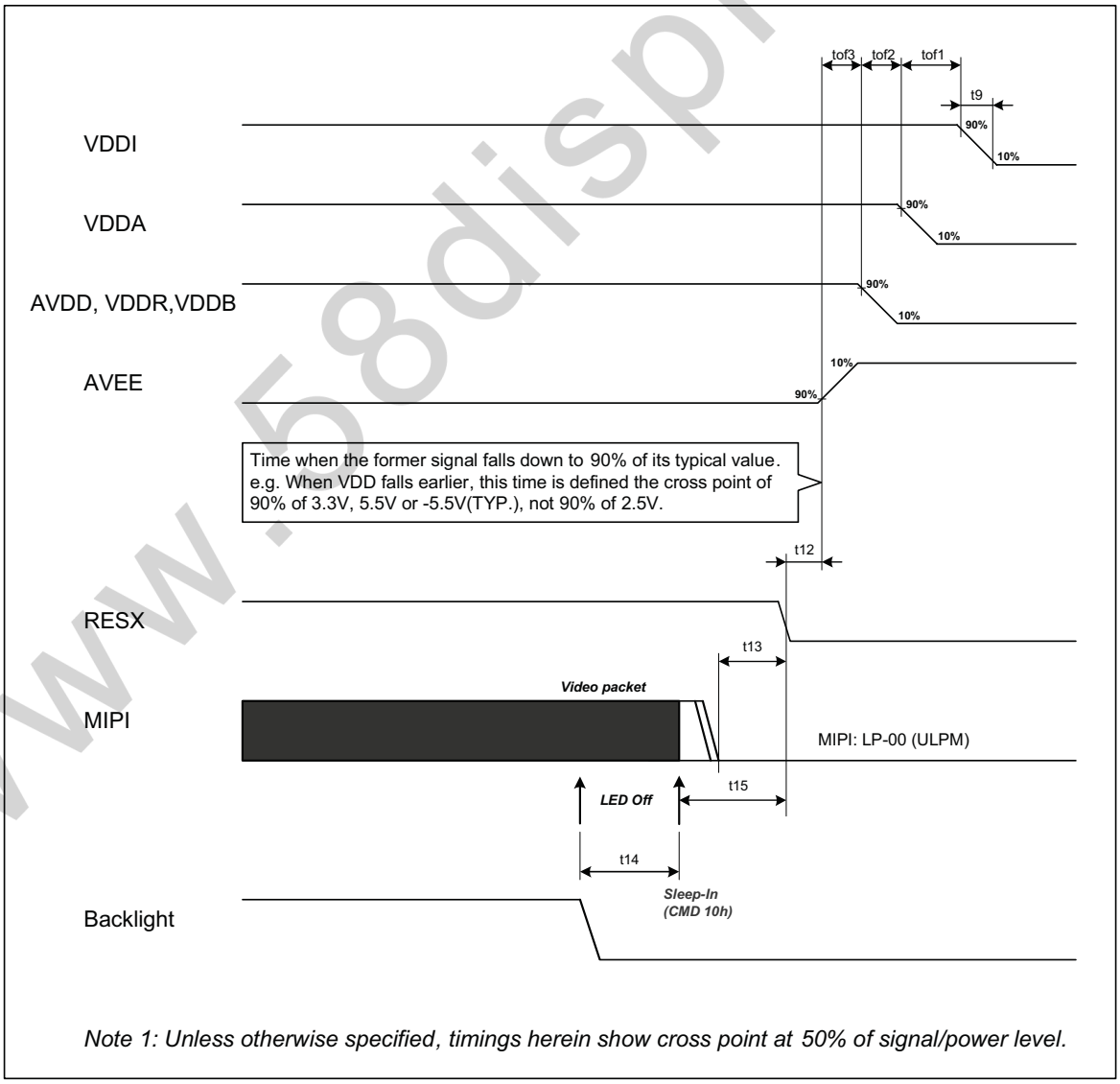
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	0	-	-	ms	
ton3	0	-	-	ms	
ton4	0	-	-	ms	
t2	-	No limit	-	µs	
t4	40	-	-	ms	
t5	20	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	µs	
t8	8	-	-	VS	Keep data more than 8 frames (VS)

Note: 1 frame=16.67ms

b. Power off:

VDDI (V18)=1.7~1.9V, VDDA (V33)= 3.0~3.6V ;

The sequences of AVDD=4.5~6.0V and AVEE=-4.5~-6.0V are only for reference



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1	0	-	-	ms	
tof2	0	-	-	ms	
tof3	0	-	-	ms	
tof4	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100	-	-	ms	

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

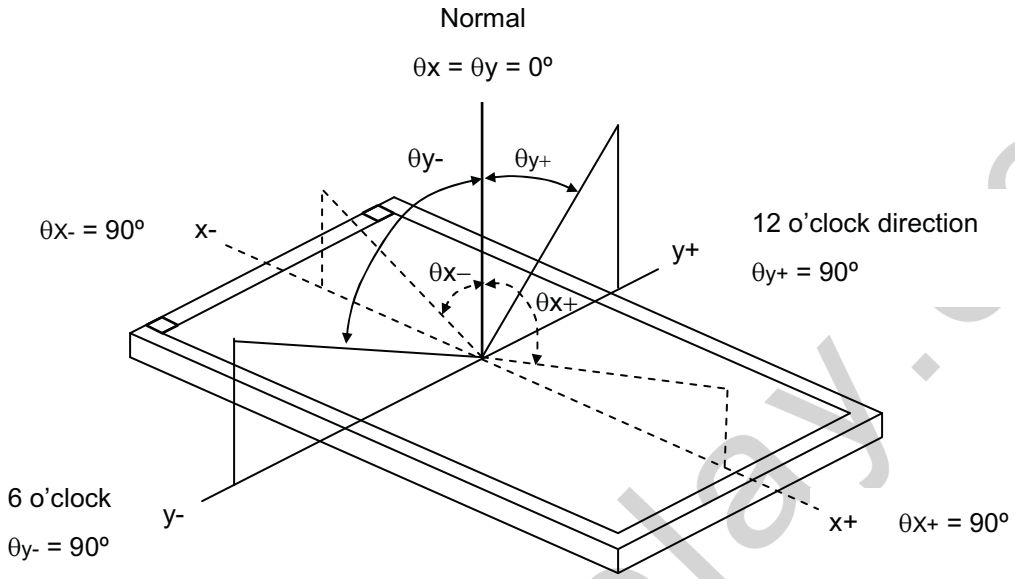
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "4.3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	120	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θY =0° Viewing Normal Angle	600	800	-	-	(2), (5) ,(7)
Response Time		TR		-	11	14	ms	(3) ,(7)
		TF		-	9	11	ms	
CP Luminance of White		LCP		340	400	-	Cd/m2	(4), (6) ,(7)
Color Coordinate	White	Wx		Typ. -0.03	0.313	Typ. +0.03	-	
		Wy			0.329		-	
	R	Rx			0.593			
		Ry			0.339			
	G	Gx			0.311			
		Gy			0.594			
	B	Bx			0.151			
		By			0.061			
NTSC		%		55	60			
Viewing Angle	Horizontal	θ_{X+}		85	89		Deg.	(1),(5) , (7)
		θ_{X-}		85	89	-		
	Vertical	θ_{Y+}		85	89	-		
		θ_{Y-}		85	89	-		
Flicker		dB	θx=0°, θY =0° Viewing Normal Angle			-28		(8)
Crosstalk		%				2		(9)
Gamma				2.0	2.2	2.4		
White Variation of 9 Points		δW_{9p}		70	-	-	%	(5),(6) , (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression：

Contrast Ratio (CR) = L255 / L0

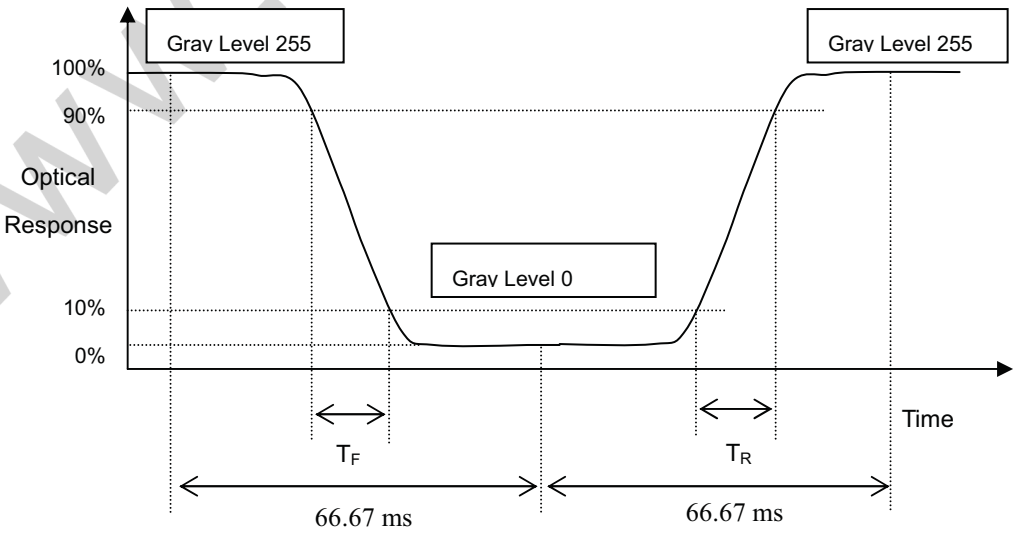
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Center Point Luminance of White (L_{CP}):

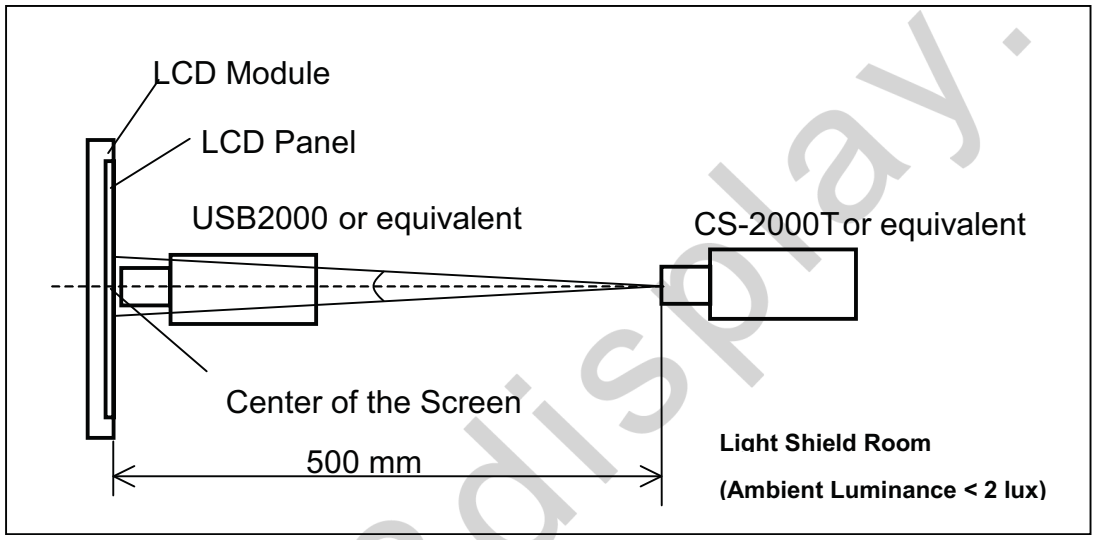
Measure the luminance of gray level 255 at center point

L_{CP} = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

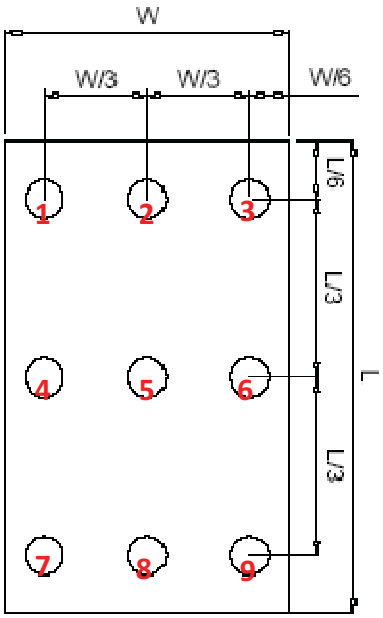
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 9 points

δW_{9p} = {Minimum [L (1) ~ L (9)] / Maximum [L (1) ~ L (9)]}*100%



Ⓧ : Test Point

X=1 to 9

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note(8) Flicker

No visual flicker will be allowed. The flicker level should be measured on GS127, The output signal is measured by Minolta CA210 immediately while Vcom is optimized. The flicker is essentially a ratio of the Amplitude in the frequency spectrum at 30 Hz (A30) and 0 Hz (A0), i.e.,

$$F = 20 \text{ Log } (A30 / A0).$$

Note(9) Crosstalk

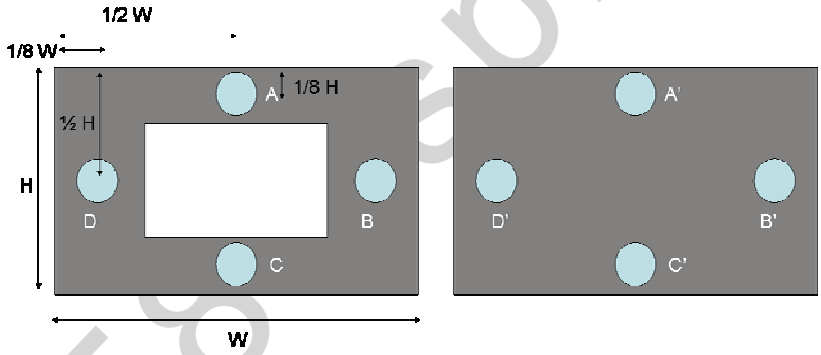
No visual cross-talk will be allowed. Two luminance values are measured at the same position (i.e. A and A'). The cross-talk, is defined as,

$$C(A, B, C, D)=| (L(A', B', C', D') – L(A, B, C, D))/L(A, B, C, D) | • 100\%,$$

Where, L(A, B, C, D) = Luminance in Position A, B, C, D

L(A', B', C', D') = Luminance in Position A', B', C', D'

Crosstalk=max (C(A), C(B), C(C), C(D))



Background : GS 127

Center Pattern: GS 255, 1/2(W) x 1/2(H).

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Operation Test	60ºC, RH 90%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±12KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) Criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hours.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N070ICE – G02

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- INX Internal Use
- Revision
- INX Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

(1)Box Dimensions : 435(L)*350(W)*275(H)
(2)60 Modules/Carton

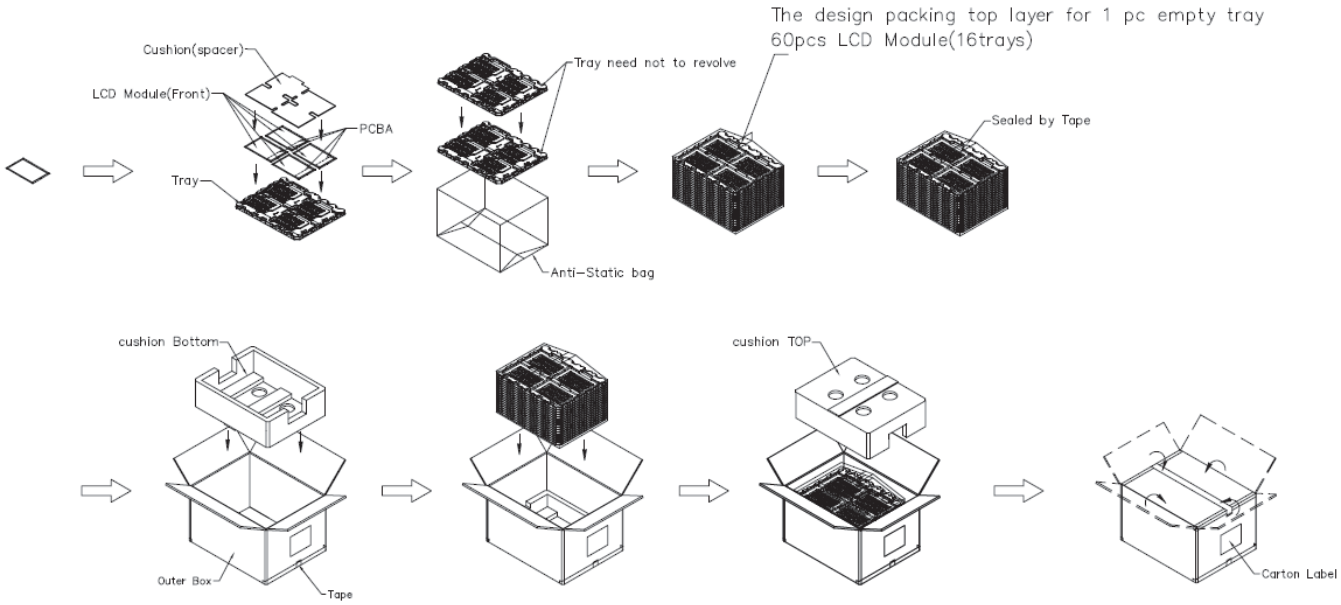


Figure. 7-1 Packing method

7.3 PALLET

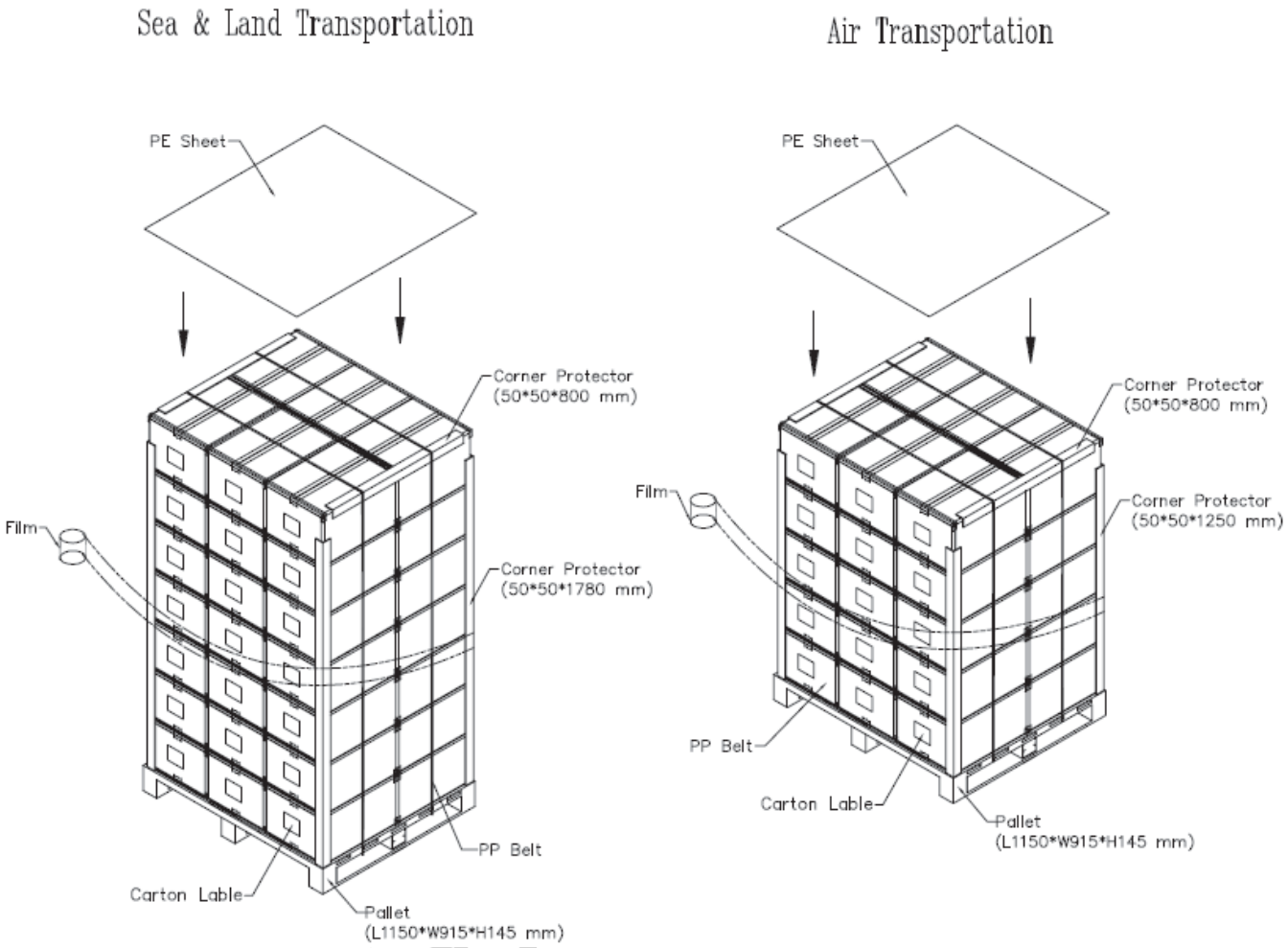


Figure. 7-2 Packing method

7.4 UN-PACKAGING METHOD

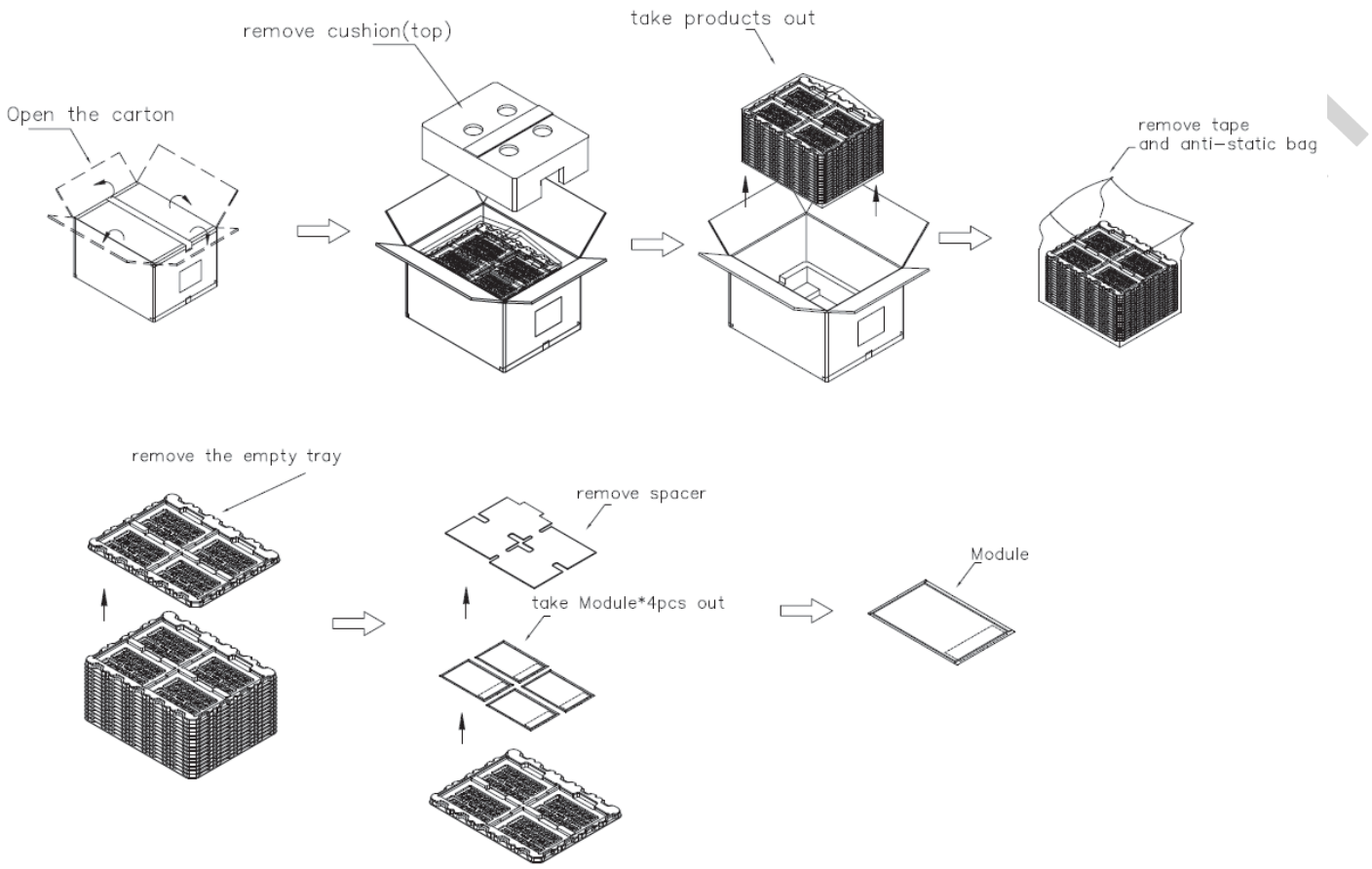


Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly.

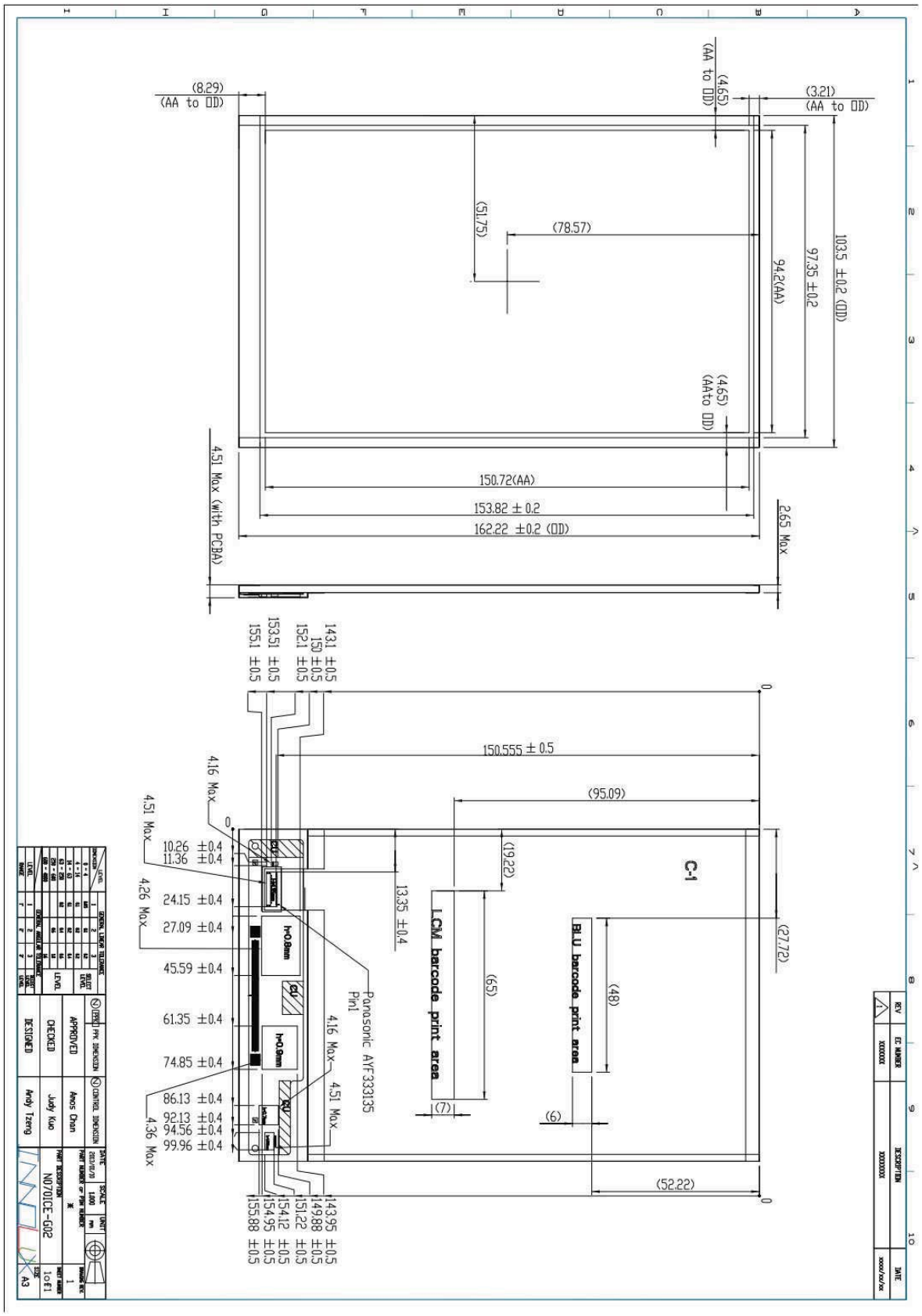
8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) Do not disassemble the module or insert anything into the Backlight unit.

Appendix 1：OUTLINE DRAWING



Appendix 2：NT35521 REGISTER SETTING (Used by MIPI LP-command)

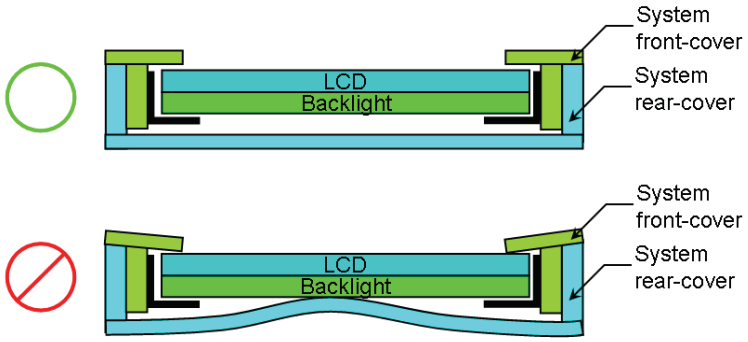
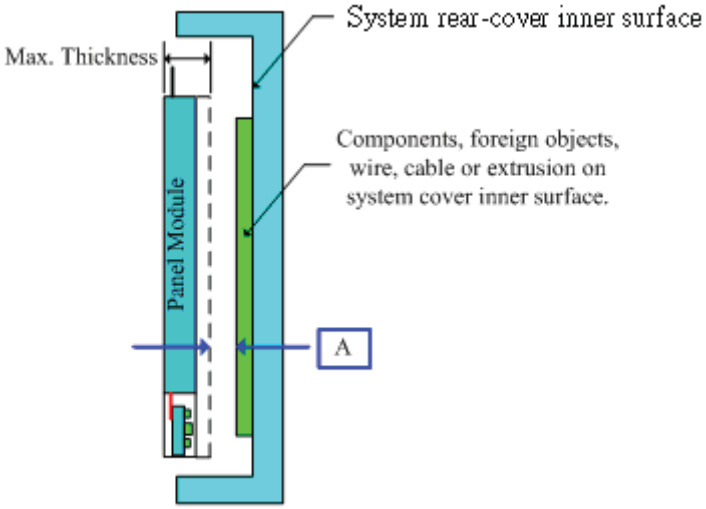
```
regw  0xFF,0xAA,0x55,0xA5,0x80
regw  0x6F,0x11,0x00
regw  0xF7,0x20,0x00
regw  0x6F,0x06
regw  0xF7,0xA0
regw  0x6F,0x19
regw  0xF7,0x12
regw  0xF0,0x55,0xAA,0x52,0x08,0x00
regw  0xC8, 0x80
regw  0xB1,0x6C,0x01
regw  0xB6,0x08
regw  0x6F,0x02
regw  0xB8,0x08
regw  0xBB,0x54,0x54
regw  0xBC,0x05,0x05
regw  0xC7,0x01
regw  0xBD, 0x02,0xB0,0x0C,0x0A,0x00
regw  0xF0,0x55,0xAA,0x52,0x08,0x01
regw  0xB0,0x05,0x05
regw  0xB1,0x05,0x05
regw  0xBC,0x8E,0x00
regw  0xBD,0x92,0x00
regw  0xCA,0x00
regw  0xC0,0x04
regw  0xB3,0x19,0x19
regw  0xB4,0x12,0x12
regw  0xB9,0x24,0x24
regw  0xBA,0x14,0x14
regw  0xF0,0x55,0xAA,0x52,0x08,0x02
regw  0xEE,0x02
regw  0xEF,0x09,0x06,0x15,0x18
regw 0xB0,0x00,0x00,0x00,0x11,0x00,0x27
regw 0x6F,0x06
regw 0xB0,0x00,0x36,0x00,0x45,0x00,0x5F
regw 0x6F,0x0C
regw 0xB0,0x00,0x74,0x00,0xA5
regw 0xB1,0x00,0xCF,0x01,0x13,0x01,0x47
regw 0x6F,0x06
regw 0xB1,0x01,0x9B,0x01,0xDF,0x01,0xE1
```

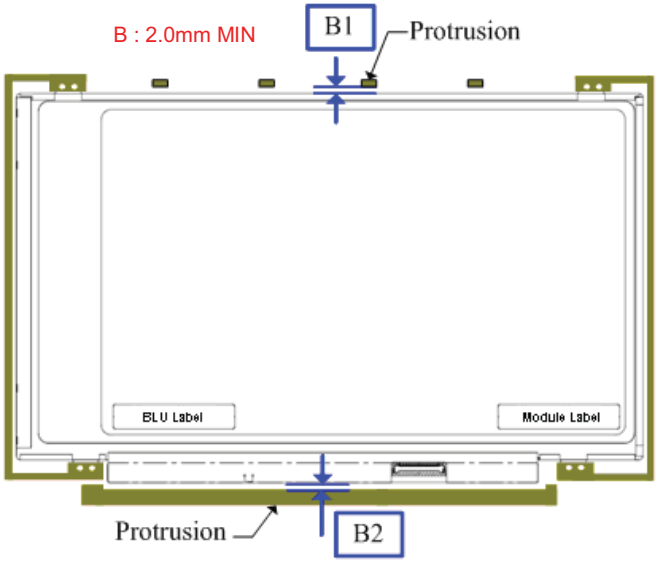
```
regw 0x6F,0x0C
regw 0xB1,0x02,0x23,0x02,0x6C
regw 0xB2,0x02,0x9A,0x02,0xD7,0x03,0x05
regw 0x6F,0x06
regw 0xB2,0x03,0x42,0x03,0x68,0x03,0x91
regw 0x6F,0x0C
regw 0xB2,0x03,0xA5,0x03,0xBD
regw 0xB3,0x03,0xD7,0x03,0xFF
regw 0xBC,0x00,0x00,0x00,0x11,0x00,0x27
regw 0x6F,0x06
regw 0xBC,0x00,0x38,0x00,0x47,0x00,0x61
regw 0x6F,0x0C
regw 0xBC,0x00,0x78,0x00,0xAB
regw 0xBD,0x00,0xD7,0x01,0x1B,0x01,0x4F
regw 0x6F,0x06
regw 0xBD,0x01,0xA1,0x01,0xE5,0x01,0xE7
regw 0x6F,0x0C
regw 0xBD,0x02,0x27,0x02,0x70
regw 0xBE,0x02,0x9E,0x02,0xDB,0x03,0x07
regw 0x6F,0x06
regw 0xBE,0x03,0x44,0x03,0x6A,0x03,0x93
regw 0x6F,0x0C
regw 0xBE,0x03,0xA5,0x03,0xBD
regw 0xBF,0x03,0xD7,0x03,0xFF
regw   0xF0, 0x55,0xAA,0x52,0x08,0x06
regw   0xB0, 0x00,0x17
regw   0xB1, 0x16,0x15
regw   0xB2, 0x14,0x13
regw   0xB3, 0x12,0x11
regw   0xB4, 0x10,0x2D
regw   0xB5, 0x01,0x08
regw   0xB6, 0x09,0x31
regw   0xB7, 0x31,0x31
regw   0xB8, 0x31,0x31
regw   0xB9, 0x31,0x31
regw   0xBA, 0x31,0x31
regw   0xBB, 0x31,0x31
regw   0xBC, 0x31,0x31
regw   0xBD, 0x31,0x09
regw   0xBE, 0x08,0x01
regw   0xBF, 0x2D,0x10
```

```
regw  0xC0, 0x11,0x12
regw  0xC1, 0x13,0x14
regw  0xC2, 0x15,0x16
regw  0xC3, 0x17,0x00
regw  0xE5, 0x31,0x31
regw  0xC4, 0x00,0x17
regw  0xC5, 0x16,0x15
regw  0xC6, 0x14,0x13
regw  0xC7, 0x12,0x11
regw  0xC8, 0x10,0x2D
regw  0xC9, 0x01,0x08
regw  0xCA, 0x09,0x31
regw  0xCB, 0x31,0x31
regw  0xCC, 0x31,0x31
regw  0xCD, 0x31,0x31
regw  0xCE, 0x31,0x31
regw  0xCF, 0x31,0x31
regw  0xD0, 0x31,0x31
regw  0xD1, 0x31,0x09
regw  0xD2, 0x08,0x01
regw  0xD3, 0x2D,0x10
regw  0xD4, 0x11,0x12
regw  0xD5, 0x13,0x14
regw  0xD6, 0x15,0x16
regw  0xD7, 0x17,0x00
regw  0xE6, 0x31,0x31
regw  0xD8, 0x00,0x00,0x00,0x00,0x00
regw  0xD9, 0x00,0x00,0x00,0x00,0x00
regw  0xE7, 0x00
regw  0xF0, 0x55,0xAA,0x52,0x08,0x03
regw  0xB0, 0x20,0x00
regw  0xB1, 0x20,0x00
regw  0xB2, 0x05,0x00,0x42,0x00,0x00
regw  0xB6, 0x05,0x00,0x42,0x00,0x00
regw  0xBA, 0x53,0x00,0x42,0x00,0x00
regw  0xBB, 0x53,0x00,0x42,0x00,0x00
regw  0xC4, 0x40
regw  0xF0, 0x55,0xAA,0x52,0x08,0x05
regw  0xB0, 0x17,0x06
regw  0xB8, 0x00
regw  0xBD, 0x03,0x01,0x01,0x00,0x01
```

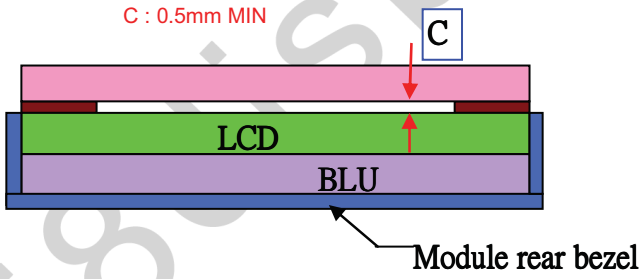
```
regw  0xB1, 0x17,0x06
regw  0xB9, 0x00,0x01
regw  0xB2, 0x17,0x06
regw  0xBA, 0x00,0x01
regw  0xB3, 0x17,0x06
regw  0xBB, 0x0A,0x00
regw  0xB4, 0x17,0x06
regw  0xB5, 0x17,0x06
regw  0xB6, 0x14,0x03
regw  0xB7, 0x00,0x00
regw  0xBC, 0x02,0x01
regw  0xC0, 0x05
regw  0xC4, 0xA5
regw  0xC8, 0x03,0x30
regw  0xC9, 0x03,0x51
regw  0xD1, 0x00,0x05,0x03,0x00,0x00
regw  0xD2, 0x00,0x05,0x09,0x00,0x00
regw  0xE5, 0x02
regw  0xE6, 0x02
regw  0xE7, 0x02
regw  0xE9, 0x02
regw  0xED, 0x33
regw  0x11
regw  0x29
```

Appendix 3： SYSTEM COVER DESIGN GUIDANCE

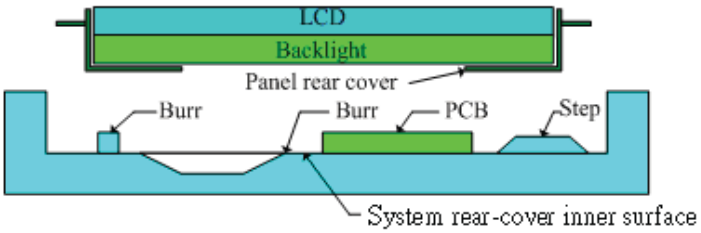
1.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
3	**Design gap B1 & B2 between panel & protrusions**



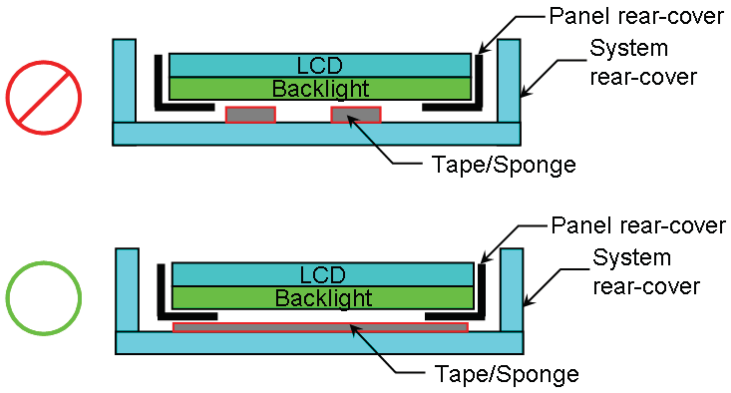
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
4	**Design gap C between touch panel & panel surface.**



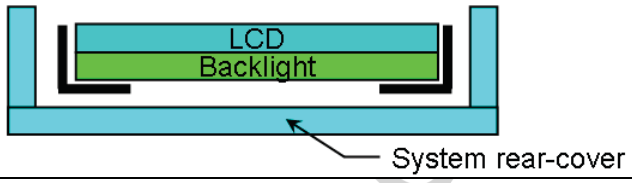
Definition	Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure. To remain sufficient gap between touch panel and panel surface is recommended.
5	**System rear-cover inner surface examination**



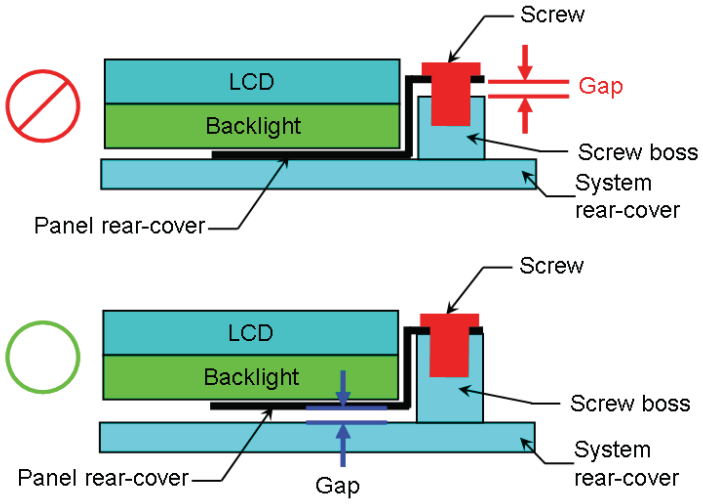
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6	**Tape/sponge design on system inner surface**



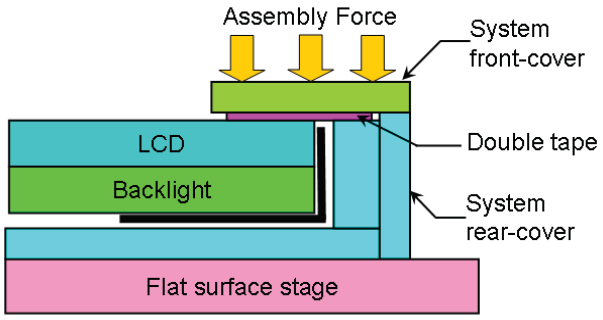
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7	**Material used for system rear-cover**



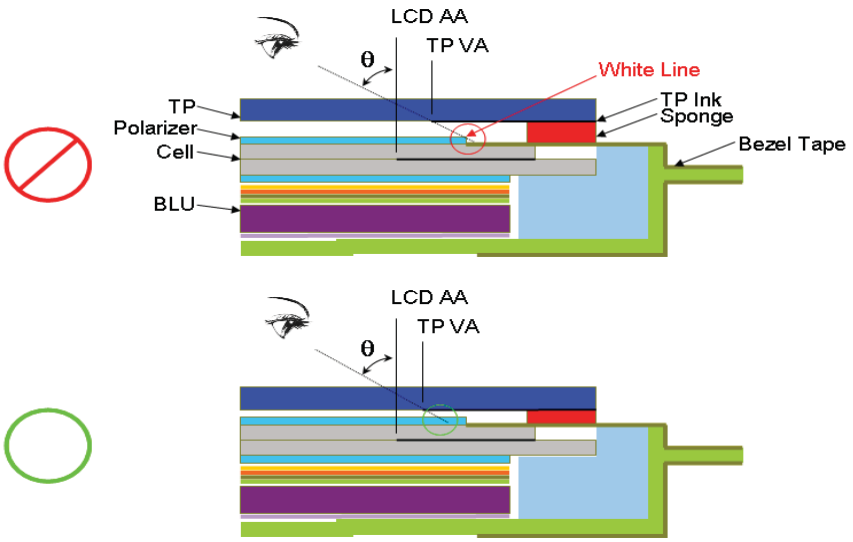
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
8	**Screw boss height design**



Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
9	**Assembly SOP examination for touch panel with double side tape design**

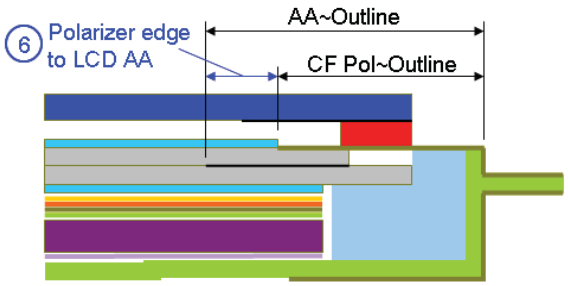


Definition	To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.
10	**Touch Application : TP and LCD Module Combination for White Line Prevention**

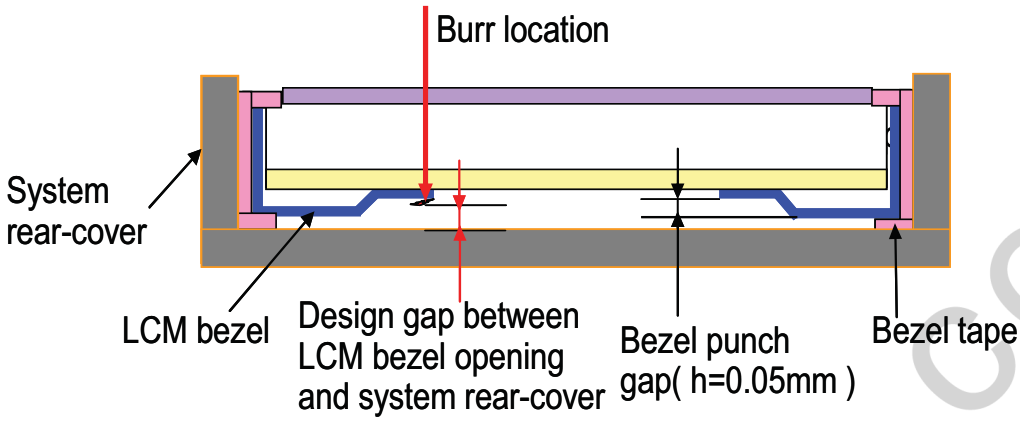


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk feasibility for your reference.
11	**System rear-cover inner surface structure for bezel opening design of module**



Definition	Burr located at bezel opening area may cause stress concentration. White spot or glass broken issue may occur during T/P lamination or system rear-cover assembly.